Customer No.: 31561
Application No.: 10/604,980
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In The Claims:

Claim 1. (original) A method of forming a pixel structure, comprising the steps of:

forming a gate and a scan line having connection with the gate over a substrate;

forming an insulation layer over the substrate covering the gate and the scan line;

forming a channel layer over the insulation layer above the gate;

forming source/drain terminals over the channel layer and a data line having connection with one of the source/drain terminals over the insulation layer, wherein the gate, the channel layer and the source/drain terminal together constitute a thin film transistor;

forming a passivation layer over the substrate covering the thin film transistor;

forming a photoresist layer over the passivation layer;

conducting a back exposure process using the source/drain terminals, the scan line and the data line as a mask and chemically developing the photoresist layer to form a patterned photoresist layer;

etching the passivation layer and the insulation layer using the patterned photoresist layer as an etching mask to expose a sidewall of the source/drain terminal;

removing the patterned photoresist layer; and

forming a pixel electrode over the passivation layer, wherein the pixel electrode and the drain terminal are electrically connected through the sidewall of the drain terminal.

Claim 2. (original) The method of claim 1, wherein before forming the pixel electrode, further includes forming an opening that exposes the drain terminal in the passivation layer such

that the pixel electrode and the drain terminal are electrically connected through conductive material within the opening as well as the sidewall of the drain terminal.

Claim 3. (original) The method of claim 1, wherein the step of forming the source/drain terminals further includes forming a conductive layer over a neighboring scan line next to the original scan line such that the conductive layer, the neighboring scan line and the insulation layer between the conductive layer and the neighboring scan line together form a pixel storage capacitor.

Claim 4. (original) The method of claim 3, wherein the pixel electrode and a sidewall of the conductive layer are electrically connected.

Claim 5. (original) The method of claim 1, wherein the data line extends towards the edge of the substrate and connects with a patterned metallic pad such that the pixel electrode and a sidewall of the metallic pad are electrically connected.

Claim 6. (original) The method of claim 1, wherein the scan line extends towards the edge of the substrate and connects with a patterned metallic pad such that the pixel electrode and a sidewall of the metallic pad are electrically connected.

Claim 7. (original) The method of claim 1, wherein after the step of forming a channel layer over the insulation layer, further includes forming an ohmic contact layer over the channel layer.

Claim 8. (original) The method of claim 1, wherein after the step of forming a channel layer over the insulation layer, further includes forming an etching stop layer over the channel layer.

Claim 9. (original) A method of forming a pixel structure, comprising the steps of:

forming a gate and a scan line having connection with the gate over a substrate;

forming an insulation layer over the substrate covering the gate and the scan line;

forming a channel material layer over the insulation layer;

forming a metallic layer over the channel layer;

forming a patterned first photoresist layer over the metallic layer;

patterning the metallic layer using the first photoresist layer as a mask to form a data line and a source/drain metallic layer;

patterning the channel material layer using the first photoresist layer as a mask to form a channel layer;

patterning the source/drain metallic layer using the first photoresist layer as a mask to form source/drain terminals, wherein the source terminal and the data line are electrically connected, and the gate, the channel layer and the source/drain terminals together constitute a thin film transistor;

removing the first photoresist layer;

forming a passivation layer over the substrate covering the thin film transistor;

forming a second photoresist layer over the passivation layer;

conducting a back exposure process using the gate, the source/drain terminals, the scan line and the data line as a mask and chemically developing the second photoresist layer to form a patterned second photoresist layer;

patterning the passivation layer and the insulation layer using the patterned second photoresist layer as a mask to expose a sidewall of the source/drain terminal;

removing the patterned second photoresist layer; and

forming a pixel electrode over the passivation layer, wherein the pixel electrode and the drain terminal are electrically connected through a sidewall of the drain terminal.

Claim 10. (original) The method of claim 9, wherein before forming the pixel electrode, further includes forming an opening that exposes the drain terminal in the passivation layer such that the pixel electrode and the drain terminal are electrically connected a through conductive material within the opening as well as the sidewall of the drain terminal.

Claim 11. (original) The method of claim 9, wherein the step of forming the source/drain terminals further includes forming a conductive layer over a neighboring scan line next to the original scan line such that the conductive layer, the neighboring scan line and the insulation layer between the conductive layer and the neighboring scan line together form a pixel storage capacitor.

Claim 12. (original) The method of claim 11, wherein the pixel electrode and a sidewall of the conductive layer are electrically connected.

Claim 13. (original) The method of claim 9, wherein the data line extends towards the edge of the substrate and connects with a patterned metallic pad such that the pixel electrode and a sidewall of the metallic pad are electrically connected.

Claim 14. (original) The method of claim 9, wherein the scan line extends towards the edge of the substrate and connects with a patterned metallic pad such that the pixel electrode and a sidewall of the metallic pad are electrically connected.

Claim 15. (original) The method of claim 9, wherein the step of patterning the source/drain terminals and the channel layer using the first photoresist layer includes the sub-steps of:

forming a patterned first photoresist layer over the metallic layer, wherein the first photoresist layer has a smaller thickness over the area above the gate than the area above the source/drain terminals and the data line;

conducting a first etching step to pattern the metallic layer into the data line and the source/drain metallic layer;

conducting a second etching step to pattern the channel material layer into the channel layer and removing a definite thickness off the first photoresist layer so that the source/drain metallic layer above the gate is exposed; and

conducting a third etching step to pattern the source/drain metallic layer into a source/drain terminal and removing a definite thickness off the channel layer.

Claim 16. (original) The method of claim 9, wherein after the step of forming a channel layer over the insulation layer, further includes forming an ohmic contact layer over the channel layer.

Claim 17. (withdrawn) A pixel structure over a substrate, the pixel structure comprising:

a thin film transistor over the substrate, the thin film transistor having a gate, a channel layer and a pair of source/drain terminals;

a scan line over the substrate, the scan line and the gate being electrically connected;

a data line over the substrate, the data line and the source terminal being electrically connected;

an insulation layer over the substrate only in areas having the gate, the source/drain terminals, the data line and the scan line thereon, and the insulation layer covering the gate and the scan line;

a passivation layer over the substrate only in areas having the gate, the source/drain terminals, the data line and the scan line, and the passivation layer covering the source/drain terminals and the data line, wherein a sidewall of the source/drain terminal is exposed; and

a pixel electrode over the substrate, the pixel electrode being positioned close to the thin film transistor such that the pixel electrode and a sidewall of the drain terminal of the thin film transistor are electrically connected.

Claim 18. (withdrawn) The pixel structure of claim 17, wherein the pixel structure further include a conductive structure within the passivation layer such that the pixel electrode and the

drain terminal are electrically connected through the conductive structure as well as the sidewall of the drain terminal.

Claim 19. (withdrawn) The pixel structure of claim 17, wherein the pixel structure further include a conductive layer over a scan line neighboring the original scan line such that the conductive layer, the neighboring scan line and the insulation layer between the conductive layer and the neighboring scan line together form a pixel storage capacitor.

Claim 20. (withdrawn) The pixel structure of claim 19, wherein a sidewall of the conductive layer is electrically connected to the pixel electrode.

Claim 21. (withdrawn) The pixel structure of claim 19, wherein the pixel structure further include a metallic pad near the edge of the substrate such that the metallic pad and the data line are electrically connected and that the pixel electrode and a sidewall of the metallic pad are electrically connected.

Claim 22. (withdrawn) The pixel structure of claim 19, wherein the pixel structure further include a metallic pad near the edge of the substrate such that the metallic pad and the scan line are electrically connected and that the pixel electrode and a sidewall of the metallic pad are electrically connected.

Claim 23. (withdrawn) The pixel structure of claim 19, wherein the pixel structure further include an ohmic contact layer over the channel layer.

Claim 24. (withdrawn) The pixel structure of claim 19, wherein the pixel structure further include an etching stop layer over the channel layer.